WHAT IS CLAIMED IS:

1. A level conversion circuit, comprising:

a first transistor of a first conductive type which is connected between a supply node to which supply voltage is impressed and an output node; and

a second transistor of a second conductive type which is connected between an input node to which an input signal is inputted and the output node,

wherein a control electrode of the second transistor is connected to the supply node and a control electrode of the first transistor is connected to an output of a prescribed circuit to which the input signal is inputted, and

wherein an output signal is obtained from the output node.

2. A level conversion circuit according to Claim 1,

wherein the single supply voltage is set for the first and second transistors or the different supply voltages are separately set for the first and second transistors,

wherein the supply voltage which corresponds to the first transistor is set to a value higher than high level of the input signal and the supply voltage which corresponds to the second transistor is set to a higher value than high level of the input signal,

wherein degree of ON status of the first and second transistors is controlled according to difference between the supply voltages and voltage of the input signal, and

wherein the input signal is converted to the output signal corresponding to the supply voltage.

3. A level conversion circuit according to Claim 1,

wherein the supply voltage is set to the higher value than the high level of the input signal,

wherein the degree of the ON status of the first transistor is controlled according to the difference between the supply voltage and the voltage of the input signal, and

wherein the input signal is converted to the output signal corresponding to the supply voltage.

4. A level conversion circuit according to Claim 1,

wherein the supply voltage is set to the higher value than the high level of the input signal,

wherein the degree of the ON status of the second transistor is controlled according to the difference between the supply voltage and the voltage of the second input signal, and

wherein the input signal is converted to the output signal corresponding to the supply voltage which acts on the first transistor.

5. A level conversion circuit according to Claim 1, wherein the control electrode of the second transistor is connected to the supply node via a control circuit which decreases the supply voltage by a prescribed value.

6. A level conversion circuit according to Claim 1, wherein the prescribed circuit is an inverter circuit.

7. A level conversion circuit according to Claim 1, wherein the control electrode of the first transistor is connected to an output of a control circuit which increases an output of the prescribed circuit by a prescribed value.

8. A level conversion circuit, comprising:

a first transistor of a first conductive type which is connected between a supply node to which supply voltage is impressed and an output node; and

a second transistor of a second conductive type which is connected between a first input node to which a first input signal is inputted and the output node,

wherein a control electrode of the second transistor is connected to the supply node and a control electrode of the first transistor is connected to a second input node to which a second input signal is inputted, while an output signal is obtained from the output node, and

wherein the control electrode of the second transistor

is connected to the supply node via a control circuit which decreases the supply voltage by a prescribed value.

9. A level conversion circuit, comprising:

a first transistor of a first conductive type which is connected between a supply node to which supply voltage is impressed and an output node; and

a second transistor of a second conductive type which is connected between a first input node to which a first input signal is inputted and the output node,

wherein a control electrode of the second transistor is connected to the supply node and a control electrode of the second transistor is connected to a second input node to which a second input signal is inputted, while an output signal is obtained from the output node, and

wherein the control electrode of the first transistor is connected to the second input node via a control circuit which increases voltage of the second input node by a prescribed value.

10. A level conversion circuit, comprising:

a first transistor of a first conductive type which is connected between a supply node to which supply voltage is impressed and a first output node;

a second transistor of a second conductive type which is connected between a first input node to which a first

input signal is inputted and the first output node;

a third transistor of the first conductive type which is connected between the supply node and a second output node; and

a fourth transistor of the second conductive type which is connected between a second input node to which a second input signal is inputted and the second output node,

wherein control electrodes of the second and fourth transistors are connected to the supply node,

wherein a control electrode of the first transistor is connected to the second output node and a control electrode of the third transistor is connected to the first output node, and

wherein an output signal is obtained from the first or second output node.

11. A level conversion circuit, comprising:

a first transistor of a first conductive type which is connected between a supply node to which supply voltage is impressed and a first output node;

a second transistor of a second conductive type which is connected between a first input node to which a first input signal is inputted and the first output node;

a third transistor of the first conductive type which is connected between the supply node and a second output node; and

a fourth transistor of the second conductive type which is connected between a second input node to which a second input signal is inputted and the second output node,

wherein a control electrode of the second transistor is connected to the second output node and a control electrode of the fourth transistor is connected to the first output node,

wherein control electrodes of the first and third transistors are respectively connected to the second and first input nodes, and

wherein an output signal is obtained from the first or second output node.

12. A level conversion circuit according to Claim 10,

wherein the single supply voltage is set for the first and second transistors or the different supply voltages are separately set for the first and second transistors,

wherein the supply voltage which corresponds to the first transistor is set to a value higher than high level of the first input signal and the supply voltage which corresponds to the second transistor is set to a higher value than high level of the second input signal,

wherein degree of ON status of the first, second, third and fourth transistors is controlled according to difference between the supply voltages and voltage of the first input signal and between the supply voltages and

voltage of second input signal, and

wherein the first input signal is converted to the output signal corresponding to the supply voltage.

13. A level conversion circuit according to Claim 11,

wherein the single supply voltage is set for the first and second transistors or the different supply voltages are separately set for the first and second transistors,

wherein the supply voltage which corresponds to the first transistor is set to a value higher than high level of the first input signal and the supply voltage which corresponds to the second transistor is set to a higher value than high level of the second input signal,

wherein degree of ON status of the first, second, third and fourth transistors is controlled according to difference between the supply voltages and voltage of the first input signal and between the supply voltages and voltage of second input signal, and

wherein the first input signal is converted to the output signal corresponding to the supply voltage.

14. A level conversion circuit according to Claim 10, wherein the control electrodes of the second and fourth transistors are connected to the supply node via a control circuit which decreases the supply voltage by a prescribed value.

15. A level conversion circuit according to Claim 11, wherein the control electrodes of the first and third transistors are connected to the second input node via a control circuit which increases voltage thereof by a prescribed value.

16. A level conversion circuit according to Claim 10, wherein a prescribed reference voltage signal is inputted as the second input signal.

17. A level conversion circuit according to Claim 11, wherein a prescribed reference voltage signal is inputted as the second input signal.

18. A level conversion circuit according to Claim 1, further comprising:

a level conversion circuit as recited in Claim 1;

a level conversion circuit as recited in Claim 1 to which an inversion signal of the input signal is inputted as the input signal; and

a differential amplifying circuit of a cross couple type which receives output signals of those two level conversion circuits as two input signals,

wherein the differential amplifying circuit has two routes for electric current which are respectively provided

with two transistors, and points in the routes respectively connecting the transistors provided in one of the two routes are connected to output nodes from which final output signals are obtained.

19. A level conversion circuit according to Claim 18, wherein an amplifying circuit of a current mirror type is provided instead of the differential amplifying circuit of the cross couple type.

20. A level conversion circuit according to Claim 8, comprising:

a level conversion circuit as recited in Claim 8;

a level conversion circuit to as recited in Claim 8 to which the first input signal and the second input signal are inputted in a mutually replaced manner; and

a differential amplifying circuit of a cross couple type which receives output signals of those two level conversion circuits as two input signals,

wherein the differential amplifying circuit has two routes for electric current which are respectively provided with two transistors, and points in the routes respectively connecting the transistors provided in one of the two routes are connected to output nodes from which final output signals are obtained.

21. A level conversion circuit according to Claim 9, comprising:

a level conversion circuit as recited in Claim 9;

a level conversion circuit as recited in Claim 9 to which the first input signal and the second input signal are inputted in a mutually replaced manner; and

a differential amplifying circuit of a cross couple type which receives output signals of those two level conversion circuits as two input signals,

wherein the differential amplifying circuit has two routes for electric current which are respectively provided with two transistors, and points in the routes respectively connecting the transistors provided in one of the two routes are connected to output nodes from which final output signals are obtained.

22. A level conversion circuit according to Claim 20, wherein an amplifying circuit of a current mirror type is provided instead of the differential amplifying circuit of the cross couple type.

23. A level conversion circuit,

wherein a first and a second transistors are connected between supply voltage and prescribed voltage in series, difference of voltage between which is larger than amplitude of an input signal, so that there might be voltage division

effect by resistors between the supply voltage and the prescribed voltage due to ON status resistance of the transistors,

wherein the first transistor becomes strong ON status and the second transistor becomes weak ON or OFF status according to difference between the voltage of the input signal and the supply voltage, when the input signal is high,

wherein the second transistor becomes strong ON status and the first transistor becomes weak ON or OFF status according to difference between the voltage of a signal inverted from the input signal and the supply voltage, when the input signal is low, and

wherein intermediate voltage generated by the voltage division effect by resistors due to the transistors is obtained as an output signal.

24. A level conversion circuit,

wherein a first and a second transistors are connected between first supply voltage and prescribed voltage in series in this order, difference of voltage between which is larger than amplitude of an input signal, so that there might be voltage division effect by resistors between the first supply voltage and the prescribed voltage due to ON status resistance of the first and second transistors,

wherein a third and a fourth transistors are connected between second supply voltage and the prescribed voltage in

series in this order, difference of voltage between which is larger than amplitude of a signal inverted from the input signal, so that there might be the voltage division effect by resistors between the second supply voltage and the prescribed voltage due to ON status resistance of the third and fourth transistors,

wherein the first and fourth transistors become strong ON status and the second and third transistors become weak ON or OFF status when the input signal is high,

wherein the second and third transistors become strong ON status and the first and fourth transistors become weak ON or OFF status when the input signal is low, and

wherein intermediate voltage generated by the voltage division effect by resistors due to the first and second transistors is utilized for controlling the third or fourth transistor and intermediate voltage generated by the voltage division effect by resistors due to the third and fourth transistors is utilized for controlling the first or second transistor and one of these intermediate voltages is obtained as an output signal.

25. A level conversion circuit according to Claim 24,

wherein the second and third transistors become the weak ON or OFF status according to difference between voltage of the input signal and the first and second supply voltages respectively when the input signal is high, and

wherein the first and fourth transistors become the weak ON or OFF status according to difference between voltage of a signal inverted from the input signal and the first and second supply voltages respectively when the input signal is low.

26. A level conversion circuit, comprising:

a p-channel field effect transistor connected between an output node and a supply node to which supply voltage that is higher than high level of an input signal is impressed;

a n-channel field effect transistor connected between a first input node to which the input signal is inputted and the output node; and

an inverter circuit which inverts the input signal,

wherein a gate of the n-channel field effect transistor is connected to the supply node and a gate of the p-channel field effect transistor is connected to an output of the inverter circuit, and

wherein an output signal is obtained from the output node.

27. A level conversion circuit, comprising:

a first transistor which is a p-channel field effect transistor connected between a first supply node to which first supply voltage is impressed and a first output node;

a second transistor which is a n-channel field effect transistor connected between a first input node to which a first input signal is inputted and the first output node;

a third transistor which is the p-channel field effect transistor connected between a second supply node to which second supply voltage is impressed and a second output node; and

a fourth transistor which is the n-channel field effect transistor connected between a second input node to which a second input signal is inputted and the second output node,

wherein gates of the second and fourth transistors are connected respectively to one of the first and second supply nodes,

wherein a gate of the first transistor is connected to the second output node and a gate of the third transistor is connected to the first output node, and

wherein an output signal is obtained from the first or second output node.

28. A level conversion circuit according to Claim 27, wherein the gates of the second and fourth transistors are respectively connected to one of the first and second supply nodes via control circuits which decrease the first or second supply voltage.

29. A level conversion circuit, comprising:

a first transistor which is a p-channel field effect transistor connected between a first supply node to which first supply voltage is impressed and a first output node,

a second transistor which is a n-channel field effect transistor connected between a first input node to which a first input signal is inputted and the first output node;

a third transistor which is the p-channel field effect transistor connected between a second supply node to which second supply voltage is impressed and a second output node; and

a fourth transistor which is the n-channel field effect transistor connected between a second input node to which a second input signal is inputted and the second output node,

wherein a gate of the second transistor is connected to the second output node and a gate of the fourth transistor is connected to the first output node,

wherein gates of the first and third transistors are connected respectively to the second and first input nodes, and

wherein an output signal is obtained from the first or second output node.

30. A level conversion circuit according to Claim 27, wherein a prescribed reference voltage signal is inputted as

the second input signal.

31. A level conversion circuit according to Claim 29, wherein a prescribed reference voltage signal is inputted as the second input signal.

32. A level conversion circuit according to Claim 1, wherein the output signal is adjusted to have target voltage Vm = (VG + VDD) / 2 as center of amplitude thereof when the ground voltage and the supply voltage are respectively described as VG and VDD.

33. A level conversion circuit according to Claim 32 characterized in that it further comprises a buffer circuit which has the target voltage Vm as a central point of operation, and amplitude of output of which covers from voltage close to the ground voltage to voltage close to the supply voltage,

wherein a modified output signal is obtained by passing the output signal through the buffer circuit.

34. A level conversion circuit according to Claim 1, wherein the transistors are made of polycrystalline silicon.

35. A level conversion circuit according to Claim 10, wherein the transistors are made of polycrystalline silicon.

36. A level conversion circuit according to Claim 11, wherein the transistors are made of polycrystalline silicon.